1. (Amended) A shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising:

flip flops of a plurality of steps that output the input pulse in synchronization with the clock signal, said flip flops being divided into a plurality of blocks, each of the blocks including at least one of said flip flops; and

a plurality of level shifters, one of the level shifters corresponding to each of the blocks, the level shifters for increasing the voltage of the clock signal and for applying the clock signal to each of said flip flops, said shift register transmitting the input pulse in synchronization with the clock signal,

wherein when one of the blocks does not require input of the clock signal, the corresponding level shifter is suspended at that point.

20. (Amended) A shift register, in which a plurality of flip flops are connected, for transmitting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising:

a plurality of level shifters for level-shifting the clock signal, wherein at least one level shifter is provided for a predetermined number of said flip flops, the level shifters for increasing the voltage of the clock signal and for applying the clock signal to each of the flip flops,

wherein when one of the level shifters does not require input of the clock signal, the corresponding level shifter is suspended at that point.

REMARKS

Applicants appreciate the courtesies extended by the Examiner to Applicants' representative during a telephone interview on February 11, 2003. During the interview, Applicants' representative explained the differences between the claimed invention and the Moriyama et al. and Ishii references.